GT74LVC595
8-Bit Shift Registers with 3-State Output Registers

1 Features

- Wide Operating Voltage Range: 1.65V to 5.5V
- Inputs Accept Voltages Higher than the Supply Voltage
- All Inputs with Schmitt-Trigger Actions
- Shift register has direct clear
- Balanced Propagation Delays
- Operation Temperature Range –40°C to +125°C, TA
- Available in Green TSSOP16 and SOP16 Packages

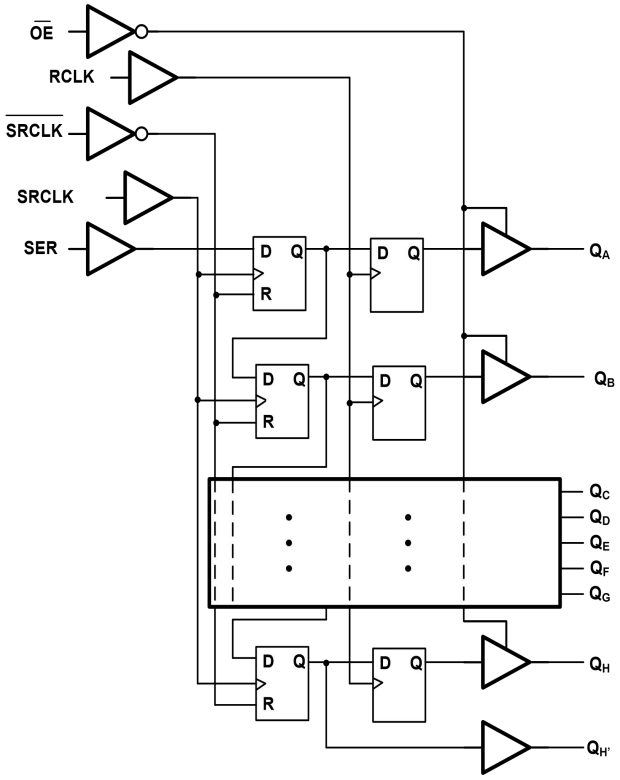
2 Application

- Output expansion
- LED matrix control
- 7-segment display control
- 8-bit data storage

3 Description

The GT74LVC595 device contains an 8-bit, serial-in,parallel-out shift register that feeds an 8-bit D-type storage register.The storage register has parallel 3-state outputs.Separate clocks are provided for both the shift and storage register.Both the shift register and storage register have separate clocks. The shift register clock (SRCLK) is positive-edge triggered. Data is shifted on the positive-going transitions of the SRCLK. The storage register clock (RCLK) is also positive-edge triggered.The data in each register is transferred to the storage register on a positive-going transition of the RCLK.The shift register has a direct overriding clear ($\overline{\text{SRCLR}}$) input,serial (SER) input, and a serial output ($Q_{H'}$) for cascading.When the output-enable ($\overline{\text{OE}}$) input is high, the storage register outputs are in a high-impedance state. Internal register data and serial output ($Q_{H'}$) are not impacted by the operation of the $\overline{\text{OE}}$ input.

Circuit Diagram



4 Revision History

Revision	Date	Note
Rev. A1. 0	2024. 04. 07	Original version

The latest datasheet version should be checked on the GTIC official website, as the company does not actively inform customers about updates to the datasheet.

5 Device Summary, Pin and Packages

Table 5-1. Device Summary(1)

Serial Name	Part Name	Package	Body Size (Nom)	Marking(2)	MSL(3)	Package Qty
GT74LVC595	GT74LVC595TE	TSSOP16	5.00mm×4.40mm×0.90mm	GT74LVC595TE XXXXXXX	3	Tape and Reel,4000
GT74LVC595	GT74LVC595PE	SOP16	9.9mm×3.9mm×1.40mm	GT74LVC595PE XXXXXXX	3	Tape and Reel,4000

(1)For all available packages, please contact product sales.

(2)There may be additional marking, which relates to the lot trace code information (data code and Vendor code), the logo or the environmental category on the device.

(3)MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

(4)"XXXXX" in Marking will be appeared as the batch code.

5 Device Summary, Pin and Packages(Continued)

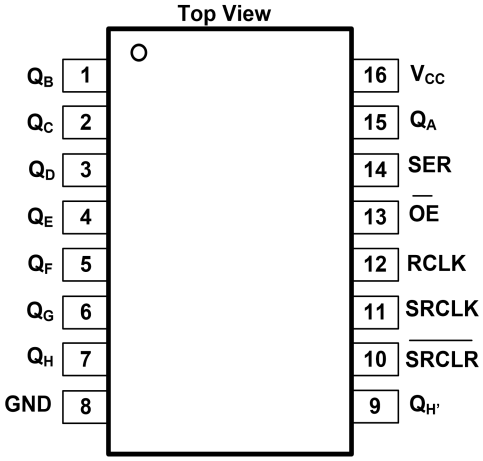


Fig.5-1 GT74LVC595: TE(TSSOP16) Package

GT74LVC595: PE(SOP16) Package

Table 5-1 Pin Definition

PIN		I/O	DESCRIPTION
NAME	NO.		
Q_B	1	O	Q_B Output
Q_C	2	O	Q_C Output
Q_D	3	O	Q_D Output
Q_E	4	O	Q_E Output
Q_F	5	O	Q_F Output
Q_G	6	O	Q_G Output
Q_H	7	O	Q_H Output
GND	8	-	Ground
$Q_{H'}$	9	O	Serial O, can be used for cascading
$\overline{SRCLR}$	10	I	Shift register clear, active low
SRCLK	11	I	Shift register clock, rising edge triggered
RCLK	12	I	O register clock, rising edge triggered
$\overline{OE}$	13	I	O Enable, active low
SER	14	I	Serial Input
Q_A	15	O	Q_A Output
VCC	16	-	Positive supply

*It is suggested to leave the unconnected pins floating.

6 Voltage, Temperature, ESD and Thermal Ratings

6.1 Absolute Maximum Ratings

Parameters			Min	Max.	Unit
V_{CC}	Supply voltage range		-0.5	6.5	V
I_{IK}	Input clamp current(1)	V_I < -0.5V	-20	20	mA
I_{OK}	Output clamp current(2)	V_O < -0.5V or V_O > V_{CC} + 0.5 V	-20		mA
V_I	Input voltage		-0.5	7	V
I_O	Output current		-25	25	mA
Icc	Continuous current through V_{CC} or GND		-75	75	mA
T_J	Junction temperature under bias			150	˚C
T_{stg}	Storage temperature range		-65	150	˚C
Soldering	Lead Temperature			260	˚C

(1)Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions.If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2)The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

ESD			Value	Unit
V(ESD)	Electrostatic discharge	Human-Body Model (HBM)	±3.5K	V
		Charged Device Model (CDM)	±2K	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6 Voltage, Temperature, ESD and Thermal Ratings(Continued)

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply Voltage		1.65	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	VCC=3 V to 3.6V		100	ns/V
		VCC=4.5 V to 5.5V		20	ns/V
T_A	Ambient temperature		-40	125	° C

6.4 Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP16	73		°C/W
TSSOP16	108		°C/W

7 Electrical Specifications

7.1 Electrical Characteristics

Full=–40°C to +125°C, Typical values are at TEMP=+25°C. (unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-level Input Voltage	V_{IH}	V_{CC}=2V		Full	1.5			V
		V_{CC}=3V		Full	2.1			
		V_{CC}=5.5V		Full	3.85			
Low-level Input Voltage	V_{IL}	V_{CC}=2V		Full			0.5	V
		V_{CC}=3V		Full			0.9	
		V_{CC}=5.5V		Full			1.65	
High-level Output Voltage	V_{OH}	V_I=V_{IH} or V_{IL}	V_{CC}=2V to 4.5V,I_O=-50 uA	Full	V_{CC}-0.1			V
			V_{CC}=3V,I_O=-4 mA	Full	2.5			
			V_{CC}=4.5V,I_O=-8 mA	Full	3.8			
Low-level Output Voltage	V_{OL}	V_I=V_{IH} or V_{IL}	V_{CC}=2V to 4.5V,I_O=50 uA	Full			0.1	V
			V_{CC}=3V,I_O=4 mA	Full			0.35	
			V_{CC}=4.5V,I_O=8 mA	Full			0.5	
Input Leakage Current	I_I	V_{CC}=0V to 5.5V,V_I=5.5V or GND		+25℃		±0.1	±0.5	μA
				FULL			±1	
Off-state Output Current	I_{OZ}	V_I= V_{IH} or V_{IL},V_O=V_{CC} or GND,V_{CC}=5.5V		+25℃		±0.1	±0.5	μA
				FULL			±1	
Supply Current	I_{CC}	V_{CC}=5.5V,V_I=V_{CC} or GND, I_O=0A		+25℃		0.1	1	μA
				FULL			5	
Input Capacitance	C_i			+25℃		6		pF

7 Electrical Specifications (Continued)

7.2 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS			TEMP	MIN(1)	TYP	MAX(1)	UNITS
Propagation Delay	t_{pd}	SRCLK to $Q_{H'}$(2)	V_{CC}=3V to 3.6V	C_L=15pF	Full				ns
				C_L=50pF	Full		10	15	
			V_{CC}=4.5V to 5.5V	C_L=15pF	Full				ns
				C_L=50pF	Full		8	10	
		RCLK to Q_n(2)	V_{CC}=3V to 3.6V	C_L=15pF	Full				ns
				C_L=50pF	Full		10.5	15	
			V_{CC}=4.5V to 5.5V	C_L=15pF	Full				ns
				C_L=50pF	Full		8	12	
		$\overline{SRCLR}$ to $Q_{H'}$(3)	V_{CC}=3V to 3.6V	C_L=15pF	Full				ns
				C_L=50pF	Full		8	15	
			V_{CC}=4.5V to 5.5V	C_L=15pF	Full				ns
				C_L=50pF	Full		6	10	
Enable Time(4)	t_{en}	$\overline{OE}$ to Q_n	V_{CC}=3V to 3.6V	C_L=15pF	Full				ns
				C_L=50pF	Full		8	12	
			V_{CC}=4.5V to 5.5V	C_L=15pF	Full				ns
				C_L=50pF	Full		7	10	
Disable Time(5)	t_{dis}	$\overline{OE}$ to Q_n	V_{CC}=3V to 3.6V	C_L=15pF	Full				ns
				C_L=50pF	Full		8	11	
			V_{CC}=4.5V to 5.5V	C_L=15pF	Full				ns
				C_L=50pF	Full		7	10	
Maximum Frequency	f_{MAX}	SRCLK or RCLK	V_{CC}=3V to 3.6V		Full				MHz
			V_{CC}=4.5V to 5.5V		Full		130		
Pulse Duration	t_w	SRCLK high or low	V_{CC}=3V to 3.6V		Full	5			ns
			V_{CC}=4.5V to 5.5V		Full	5			
		RCLK high or low	V_{CC}=3V to 3.6V		Full	5			ns
			V_{CC}=4.5V to 5.5V		Full	5			
		$\overline{SRCLR}$ low	V_{CC}=3V to 3.6V		Full	5			ns
			V_{CC}=4.5V to 5.5V		Full	5			
Setup Time	t_{su}	SER to SRCLK	V_{CC}=3V to 3.6V		Full	3			ns
			V_{CC}=4.5V to 5.5V		Full	3			
		SRCLK to RCLK	V_{CC}=3V to 3.6V		Full	5			ns
			V_{CC}=4.5V to 5.5V		Full	5			

7 Electrical Specifications (Continued)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN(1)	TYP	MAX(1)	UNITS
Hold Time	t_h	SER to SRCLK	V_{CC}=3V to 3.6V	Full	2.5			ns
			V_{CC}=4.5V to 5.5V	Full	2			
Recovery Time	t_{REC}	$\overline{SRCLR}$ to SRCLK	V_{CC}=3V to 3.6V	Full	3			ns
			V_{CC}=4.5V to 5.5V	Full	3			
Power Dissipation Capacitance(6)(7)	C_{PD}	f_i=1MHz, V_I=GND to V_{CC}		+25℃		30	60	pF

NOTES:

1.Specified by design and characterization; not production tested.

2. t_{PD} is the same as t_{PHL} and t_{PLH}.

3. t_{PD} is the same as t_{PHL} only.

4. t_{EN} is the same as t_{PZL} and t_{PZH}.

5. t_{DIS} is the same as t_{PLZ} and t_{PHZ}.

6.C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o)$.

where:

f_i = Input frequency in MHz.

f_o= Output frequency in MHz.

C_L= Output load capacitance in pF.

V_{CC} = Supply voltage in Volts.

$\Sigma(C_L \times Vcc^2 \times f_O)$= Sum of outputs.

7. All 9 outputs switching.

8 Typical Characteristics

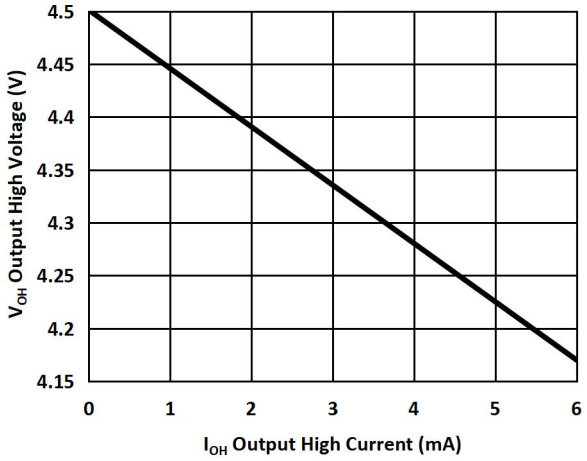


Fig.8-1 Typical Output Voltage in the High State (V_{OH})

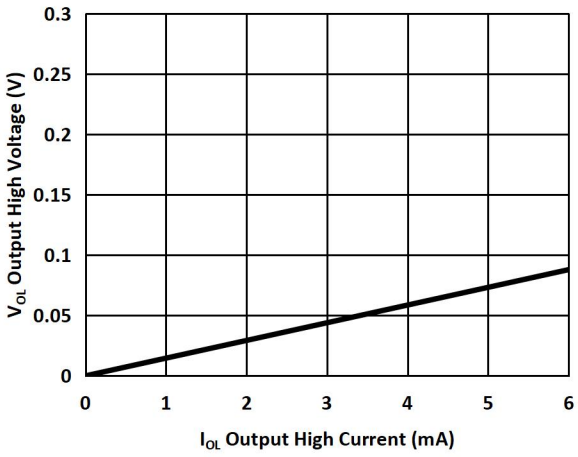


Fig.8-2 Typical Output Voltage in the Low State (V_{OL})

9 Parameter Measurement Information

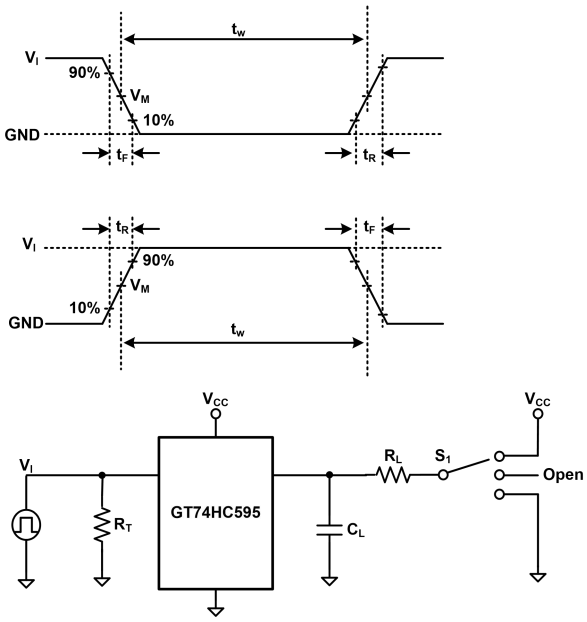


Fig.9-1 Test Circuit for Measuring Switching Times

Test conditions are given in Table 9-1.

Definitions test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_o of the pulse generator)

S_1: Test selection switch.

Tabel 9-1 Test Condition

Supply Voltage	Input		Load		S1 Position		
V_{CC}	V_I	t_R t_F	C_L	R_L	t_{PHL},t_{PLH}	t_{PZH},t_{PHZ}	t_{PZL},t_{PLZ}
1.65V to 5.5V	V_{CC}	≤3.0ns	15pF,50pF	1k	Open	GND	V_{CC}

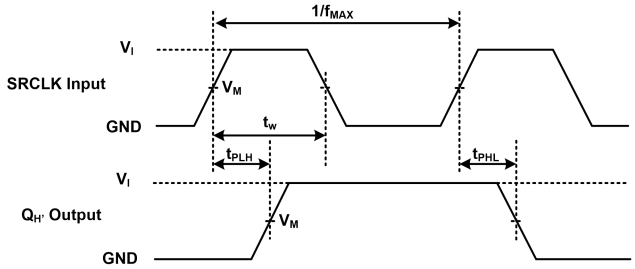


Fig.9-2 Shift Clock Pulse, Maximum Frequency and Input to Output Propagation Delays

Test conditions are given in Table 9-1.

Measurement points are given in Table 9-2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load

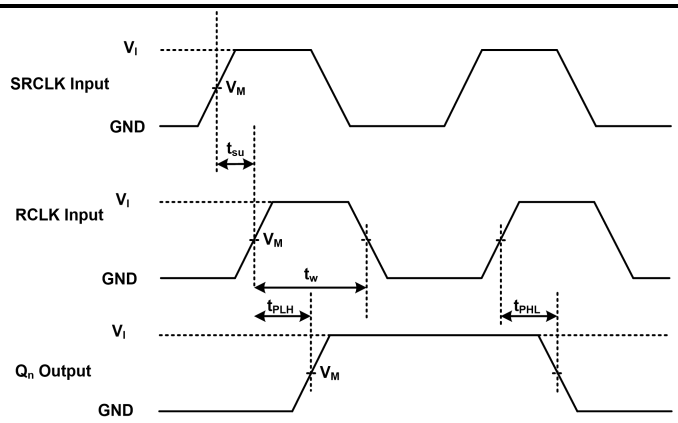


Fig.9-3 Storage Clock to Output Propagation Delays

Test conditions are given in Table 9-1.
Measurement points are given in Table 9-2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

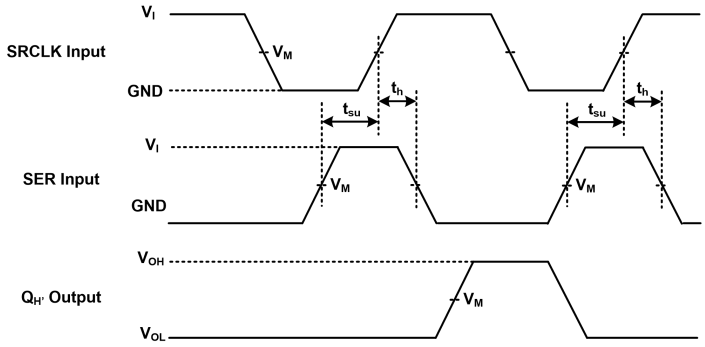


Fig.9-4 Data Set-Up and Hold Times

Test conditions are given in Table 9-1.
Measurement points are given in Table 9-2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

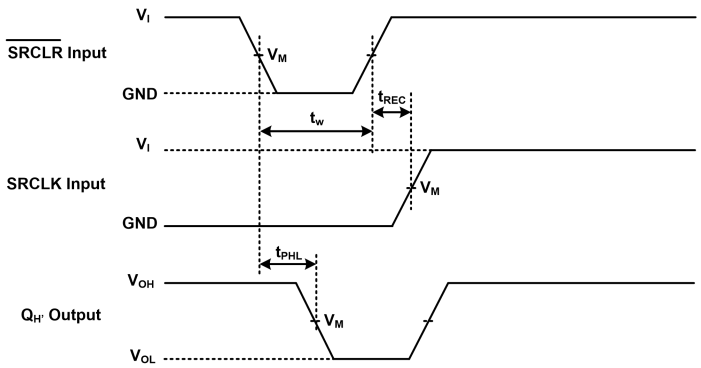


Fig.9-5 Master Reset to Output Propagation Delays

Test conditions are given in Table 9-1.
Measurement points are given in Table 9-2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

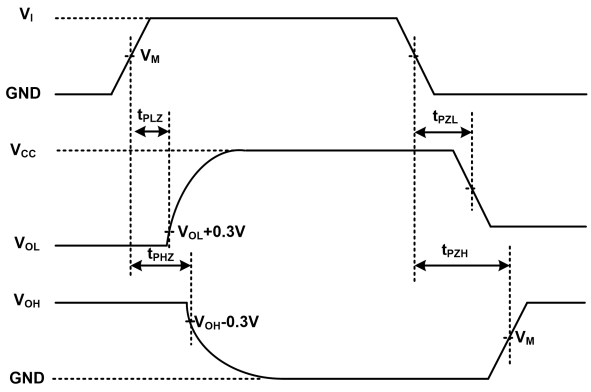


Fig.9-6 Enable and Disable Times

Test conditions are given in Table 9-1.

Measurement points are given in Table 9-2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Tabel 9-2 Measurement Points

Supply Voltage	Input	Output
V_{CC}	V_M(1)	V_M
1.65V to 5.5V	0.5×V_{CC}	0.5×V_{CC}

NOTE.

1. The measurement points should be Vim or V'i when the input rising or falling time exceeds 3.0ns.

10 Detailed Description

10.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-State outputs. The three states that these outputs can be in are driving high, driving low, and high impedance. The term balanced indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over current. The electrical and thermal limits defined in the Absolute Maximum Ratings must be followed at all times.

For the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10 kΩ resistor can be used to meet these requirements.

10.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term balanced indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over current. The electrical and thermal limits defined in the Absolute Maximum Ratings must be followed at all times.

10.3 Device Functional Modes

Table 10-1 Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled
X	X	X	X	L	Outputs Q_A – Q_H are enabled
X	X	L	X	X	Shift register is cleared
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	H	↑	X	Shift-register data is stored in the storage register
X	↑	H	↑	X	Data in shift register is stored in the storage register, the data is then shifted through.

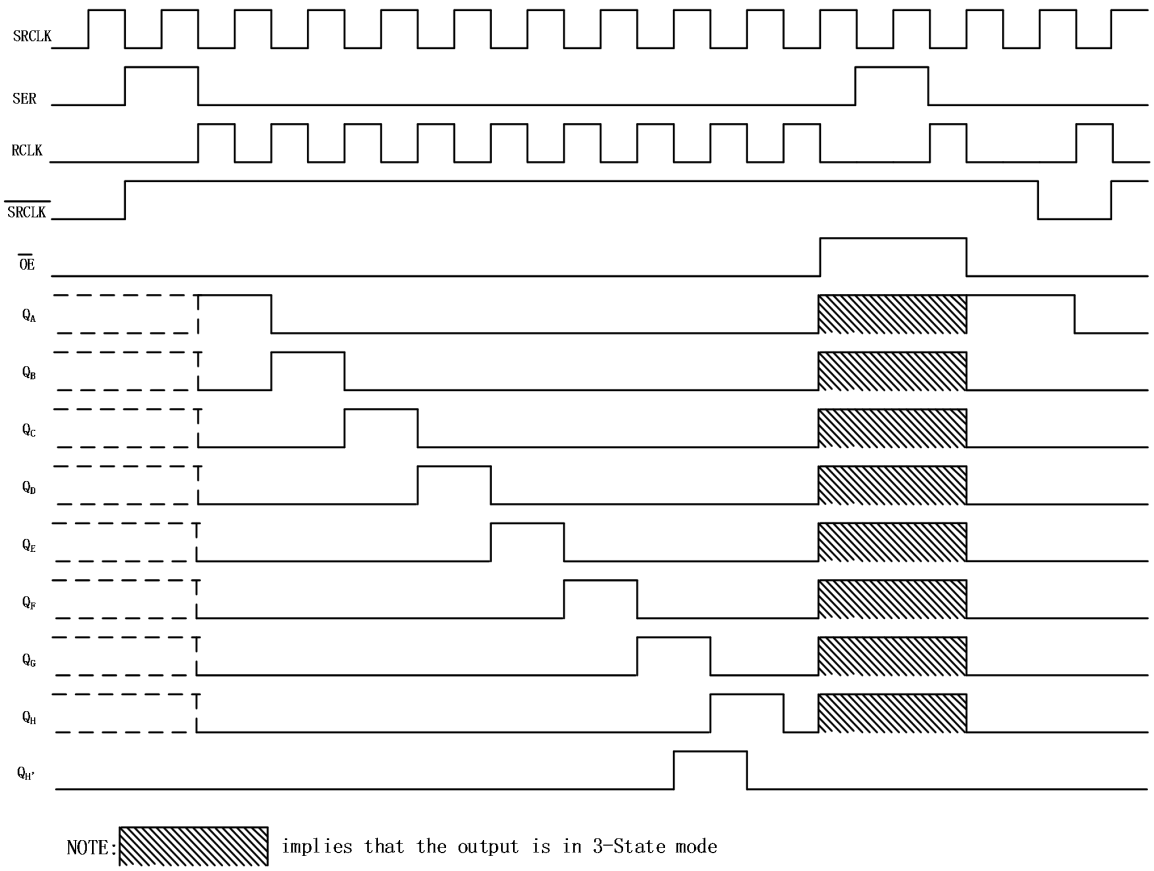


Fig.10-1 Timing Diagram

11 Application Information

In this application, the GT74LVC595 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O, the GT74LVC595 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

The OE pin is used to easily disable the outputs when the displays need to be turned off or connected to a PWM signal to control brightness. However, this pin can be tied low and the outputs of the GT74LVC595 can be controlled accordingly to turn off all the outputs reducing the I/O needed to three. There is no practical limitation to how many GT74LVC595 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register. At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, the shift register needs to be cleared and then clocked into the output register.

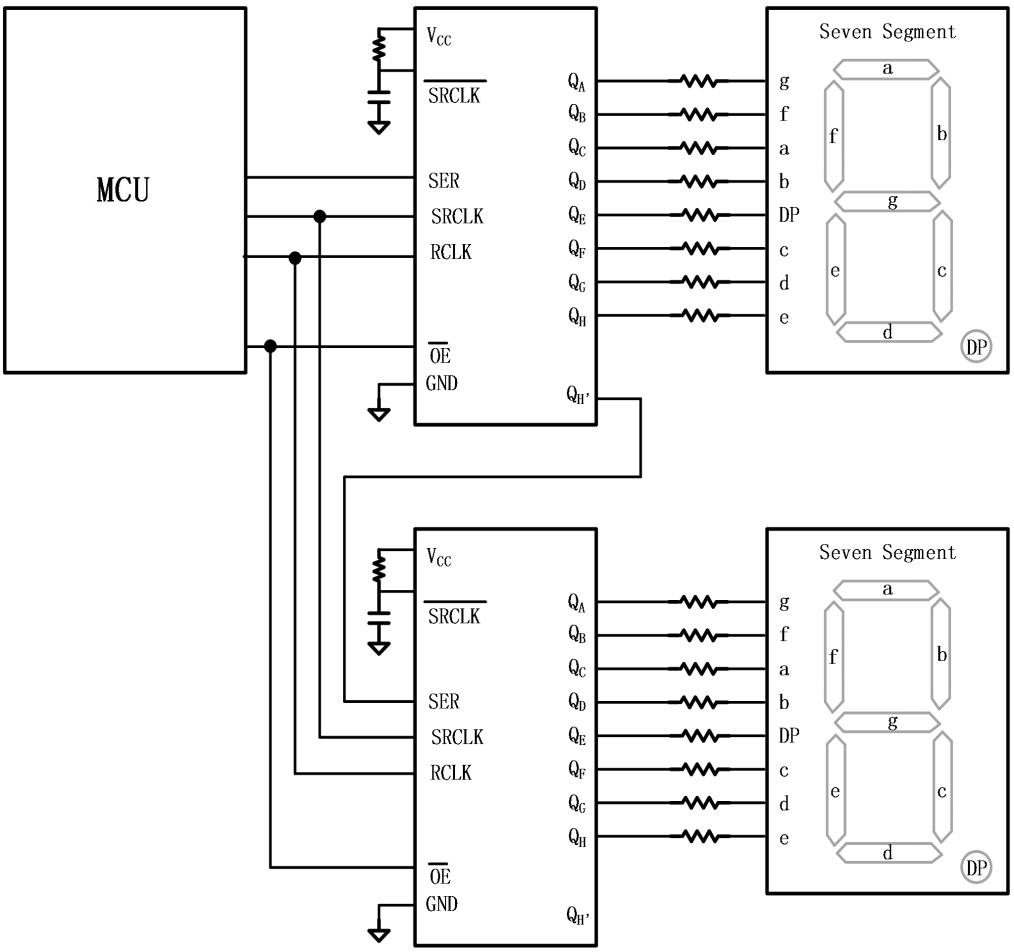
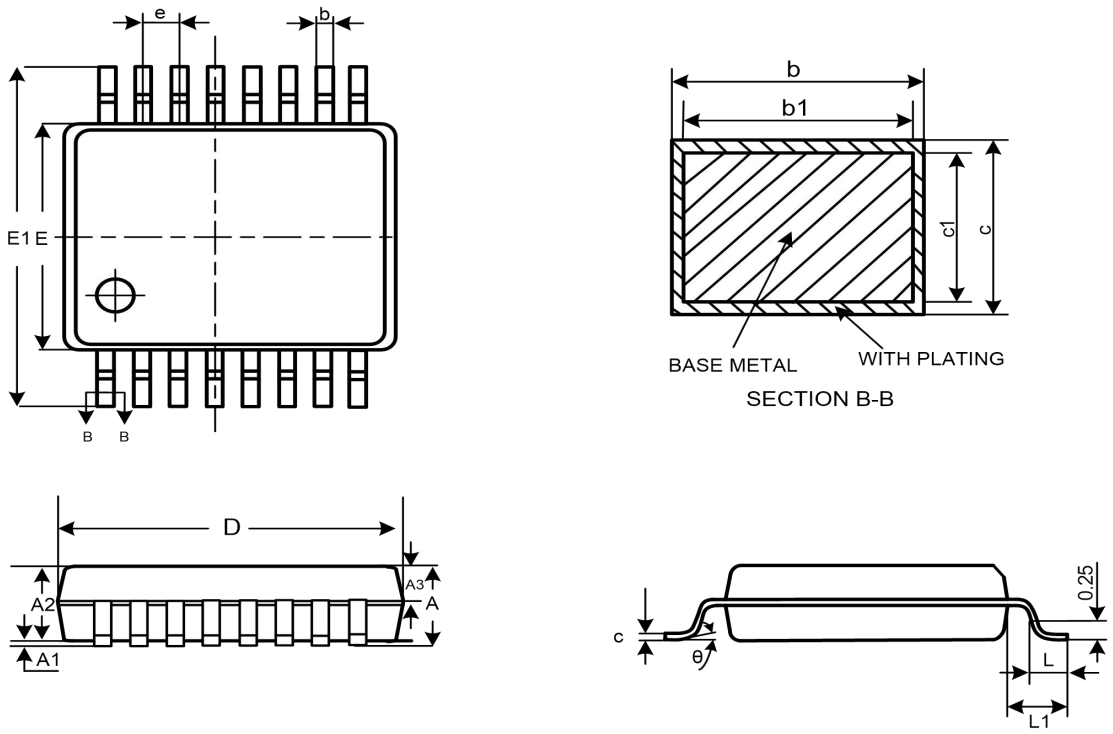


Fig.11-1 Typical Application Schematic

12 Package Outline Dimension

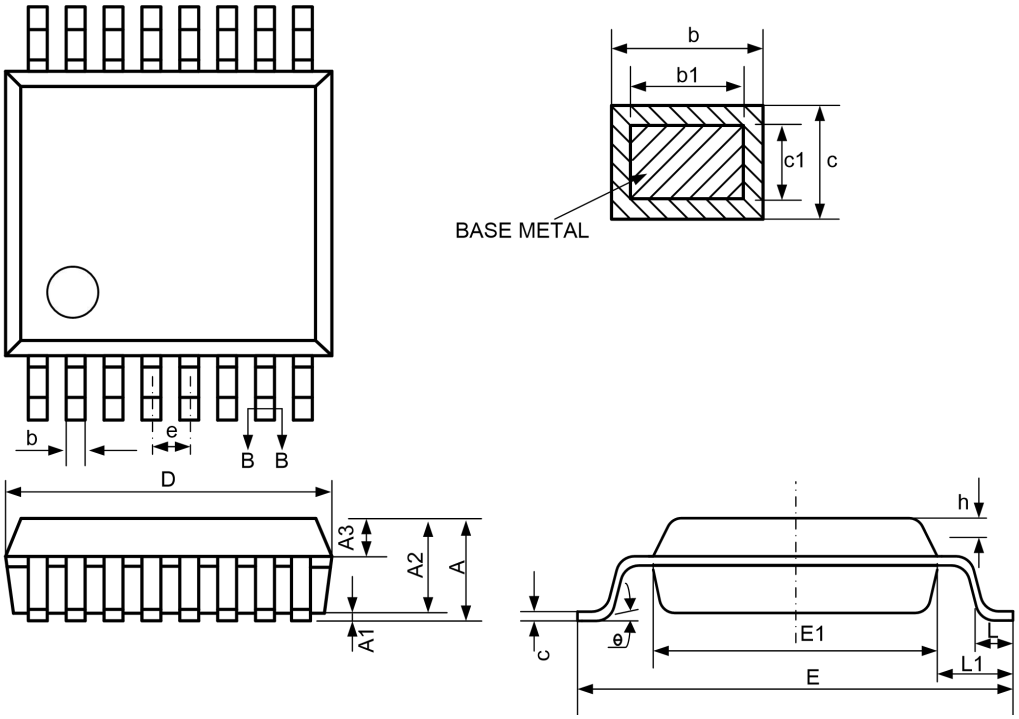
TSSOP16



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	——	——	1.20	——	——	0.047
A1	0.05	——	0.15	0.002	——	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
A3	0.39	0.44	0.49	0.015	0.017	0.019
b	0.19	——	0.30	0.007	——	0.012
b1	0.19	0.22	0.25	0.007	0.009	0.010
c	0.13	——	0.18	0.005	——	0.007
c1	0.12	0.13	0.14	0.005	0.005	0.006
D	4.86	4.98	5.10	0.191	0.196	0.201
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.260
e	0.65BSC			0.026BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00BSC			0.039BSC		
θ	0°	——	8°	0°	——	8°

12 Package Outline Dimension(Continued)

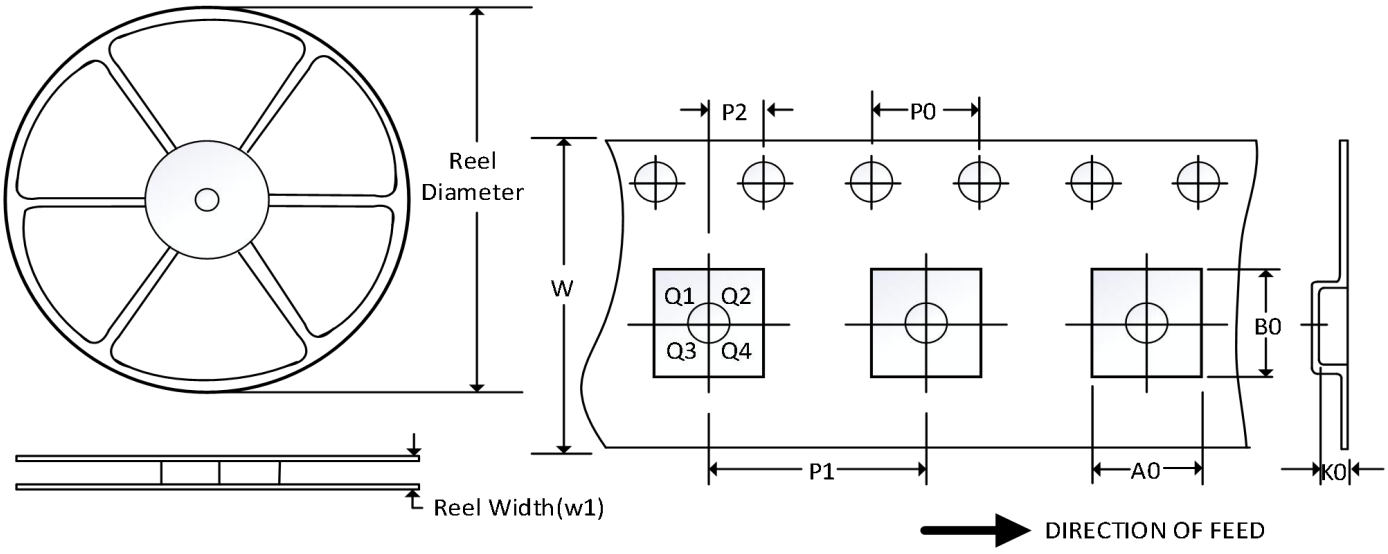
SOP16



symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	--	--	1.75	--	--	0.069
A1	0.10	--	0.225	0.004	--	0.009
A2	1.30	1.40	1.50	0.051	0.055	0.059
b	0.39	--	0.47	0.015	--	0.019
b1	0.38	0.41	0.44	0.015	0.016	0.017
c	0.20	--	0.24	0.008	--	0.009
c1	0.19	0.20	0.21	0.007	0.008	0.008
D	9.80	9.90	10.00	0.386	0.390	0.394
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27(BSC)			0.05(BSC)		
h	0.25	--	0.50	0.010	--	0.020
L	0.50	--	0.80	0.020	--	0.031
L1	1.05REF			0.041REF		
θ	0°	--	8°	0°	--	8°

13 Tape and Reel Information

Reel Dimensions **Reel Dimensions**



Note: The picture is only for reference. Please make the object as the standard.

Key Parameter List of Tape and Reel

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP16	13''	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1
SOP16	13''	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1

Note:
(1)All dimensions are nominal.
(2)Plastic or metal protrusions of 0.15mm maximum per side are not included.